

**REMARKS**

1. This paper is responsive to the Office Action mailed September 10, 2002.

Reconsideration and further examination is respectfully requested.

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2. In brief, the present invention is a method of selecting data from a computer graphics frame buffer in an efficient manner for display.

3. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

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4. Claims 1-10 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Fredrickson et al. (US 5,131,080) in view of Alcorn et al. (US 5,185,856). The Examiner contended that, "As per claim 1, Fredrickson teaches the claimed "display system" comprising: "A memory" (Fredrickson, figure 2B); and "An attribute system" (Fredrickson, column 10, lines 1-60)." However, nowhere in the lines specified by the Examiner is the applicant able to find any description of an "attribute system." In fact, the word "attribute" does not appear anywhere in that section of the Fredrickson patent, and applicant is unable to understand how this could possibly describe an "attribute system." The portion of the patent referenced appears to describe the scan converter, the pixel color data formatter, the tile address/data MUX circuit, the pixel bus, and the frame buffer controller. The frame buffer controller disclosed by Fredrickson and described in this portion of the patent controls the reading of data from the frame buffer memory. The frame buffer controller disclosed by Fredrickson includes a

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capability of “the programmability of tile sizes” allowing different shapes and sizes of the pixel tiles to be read from the frame buffer memory. Applicant is unable to find anywhere in this portion of the patent that Fredrickson claims, teaches, or suggests the use of attribute data to allow the frame buffer controller to  
5 select between a plurality of logical regions of frame buffer memory.

5. Since there appears to be some confusion about the type of attribute data included in the present invention, claims 1-4, and 7-10 have been amended to clarify that the attribute data described in the present invention is frame buffer attribute data,  
10 and is not color attribute or overlay data. Applicant believes that with this clarification claims 1 – 4, and 7 – 10 are further distinguished from the Fredrickson and Alcorn patents and are in a condition for allowance.

6. The Examiner also contended that, “Fredrickson’s (X, Y, Z) coordinate and color  
15 attributes (R, G, B) or overlay data (memory RAM 98) suggests the storing of “logical regions and attribute data” as claimed.” However, nowhere does the Fredrickson patent, claim, teach, or suggest the use of frame buffer attribute data to select which logical regions of frame buffer memory to read in displaying a given tile of pixels. In the Fredrickson patent, when a tile of pixels is to be  
20 displayed on the screen, the corresponding tile is read from all of the logical regions of memory and later calculations are performed to determine which logical region to use, then the tiles from the other logical regions are discarded, wasting the memory unit bandwidth that was used in reading data from the other logical regions. The “coordinate[s] and color attributes” referred to by the  
25 Examiner are simply the location and color of a given pixel, they have no relationship to the logical region of memory to access for a given tile of pixels.

As noted above, claims 1 – 4, and 7 – 10 have been amended to clarify that the attribute data in the applicant's invention is frame buffer attribute data, and is not coordinate or color attribute data.

- 5 7. The “overlay data” cited by the Examiner (reference character “98” in the Fredrickson patent) are described by Fredrickson (col. 2, lines 2-8) as, “Attributes include the RGB intensities, and in many systems ON and OFF for pixels in an “overlay” plane that is merged with data in other planes. For instance, an overlay plane might contain a cursor, and the presence of a bit in the overlay plane might
- 10 force saturation intensity for all three electron guns, regardless of the actual RGB values for that pixel.” Thus, what Fredrickson terms “attributes” are simply the color of a given pixel, and ON or OFF information for that pixel from the overlay data array. As described in the specification, applicant's invention uses frame buffer attribute data referring to the logical region(s) of memory to be accessed for
- 15 the display of a given tile of pixels. Within that logical region of memory are the RGB values for the pixels within the given tiles. (The overlay data is stored in a separate memory location and its location is not essential to applicant's invention.) Thus, applicant believes that the limitations of an attribute system [that] selects graphics data from fewer than all of said logical regions based on said frame
- 20 buffer attribute data are clearly distinguished from the Fredrickson patent. Further, by clarifying claims 1 – 4, and 7 – 10 that applicant's attribute data is frame buffer attribute data, applicant's invention is further distinguished from the Fredrickson and Alcorn patents.

8. The Examiner contended that, “Alcorn teaches that such attribute data is well known in the art (Alcorn, column 4, lines 29-35).” This portion of the Alcorn patent states, “The CTI simultaneously interprets a number of pixel parameters, for example, red, green and blue (RGB), specular and diffuse parameters, alpha  
5 (x,y) parameters, and texture parameters; while the ZI only interpolates x, y, and z values.” These “pixel parameters” described by Alcorn are not equivalent to applicant’s frame buffer attribute data since the “pixel parameters” do not include information regarding which subset of multiple logical regions of memory contain valid pixel data to be retrieved. Applicant is unable to find anywhere within the  
10 Alcorn patent a claim, teaching, or suggestion of an attribute system... [that] selects graphics data from fewer than all of said logical regions based on said frame buffer attribute data. As noted above, applicant has amended claims 1 – 4, and 7 – 10 to further distinguish between applicant’s frame buffer attribute data and Alcorn’s “pixel parameters.” Thus, applicant believes that claim 1 has been  
15 adequately distinguished from the Fredrickson and Alcorn patents and is in a condition suitable for allowance.

9. The Examiner also contended that, “Claim 2 adds into claim 1 that the graphics data and attribute data are stored in physically separate memory which  
20 Fredrickson teaches in figure 2B with different memory planes.” However, as discussed above, Fredrickson does not claim, teach, or suggest an attribute system ... [that] selects graphics data from fewer than all of said logical regions based on said frame buffer attribute data. Thus, while the different memory planes disclosed by Fredrickson may comprise physically separate memory devices,  
25 since Fredrickson does not disclose frame buffer attribute data capable of

distinguishing between logical regions of frame buffer memory, applicant's claims are distinguished from the invention disclosed in the Fredrickson patent.

Applicant has amended claim 2 to clarify that the attribute data in applicant's invention is frame buffer attribute data. Thus, applicant also believes that claim 2  
5 has been adequately distinguished from the Fredrickson and Alcorn patents, and is therefore in a condition suitable for allowance.


10. Claims 3-6, 7-8, and 9-10 were rejected for similar reasons to claims 1 and 2.

Applicant respectfully suggests, that since claims 1 and 2 have been distinguished  
10 from the inventions of Fredrickson and Alcorn, claims 3-6, 7-8, and 9-10 are similarly distinguished from the inventions of Fredrickson and Alcorn.

11. For these reasons, this application is considered to be in condition for allowance and such action is earnestly solicited.

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Respectfully submitted,

by 

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**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**In the claims:**

Claims 1 – 4, and 7 – 10 have been amended as follows:

- 5 1. (amended) A display system comprising:
- a memory, containing graphics data, divided into logical regions, and frame  
buffer attribute data; and
- an attribute system, connected to said memory wherein said attribute system selects  
graphics data from fewer than all of said logical regions based on said frame  
10 buffer attribute data and transmits said graphics data to a display.
2. (amended) The display system recited in claim 1; wherein said graphics data and  
said frame buffer attribute data are stored in physically separate memories.
3. (amended) A display system, comprising:
- a memory, containing graphics data, divided into logical regions, and frame  
15 buffer attribute data; and
- a regions system, that calculates which regions of said graphics data contain  
data necessary for display of a block of pixels; wherein said regions are  
fewer than all of said logical regions.
4. (amended) The display system recited in claim 3; wherein said graphics data and  
20 said frame buffer attribute data are stored in physically separate memories.
7. (amended) A method for selectively reading pixel data from a frame buffer  
memory array, comprising the steps of:
- defining a plurality of regions of frame buffer memory, wherein each region  
comprises memory to store graphics data for each pixel of a monitor;

storing frame buffer attribute data for each pixel in a memory, wherein said  
frame buffer attribute data encodes which of said regions are to be  
displayed on said monitor;

retrieving said frame buffer attribute data for a pixel from said memory;

5 calculating a subset of said regions of frame buffer memory that are required  
to display said pixel on said monitor; and

retrieving from said frame buffer memory pixel data only from said subset of  
regions of frame buffer memory that are required to display said pixel  
on said monitor.

10 8. (amended) The method for selectively reading pixel data from a frame buffer  
memory array as recited in claim 7; wherein said graphics data and said frame buffer  
attribute data are stored in said frame buffer memory.

9. (amended) A method for selectively reading pixel data from a frame buffer  
memory array, comprising the steps of:

15 defining a plurality of regions of frame buffer memory, each region further  
comprising memory to store graphics data for each pixel of a monitor;  
storing frame buffer attribute data for each pixel in a memory, encoding which  
of said regions are to be displayed on said monitor using the frame  
buffer attribute data;

20 defining groups of pixels as tiles;  
selecting a tile for display on said monitor;  
retrieving said frame buffer attribute data for said tile from said memory;  
calculating a subset of said regions of frame buffer memory that are required  
to display said tile on said monitor; and



retrieving from said frame buffer memory pixel data only from said subset of regions of frame buffer memory that are required to display said tile on said monitor.

10. (amended) The method for selectively reading pixel data from a frame buffer  
5 memory array as recited in claim 9; wherein said graphics data and said frame buffer  
attribute data are stored in said frame buffer memory.